Proposition de recherche doctorale

Reliability of Probabilistic Circuits

Mots clés :

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- **Unité de recherche** : Laboratoire Traitement et Communication de l'Information
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- **Domaine scientifique principal**: Divers

Résumé du projet de recherche (Langue 1)

The problem of computing correctness in a probabilistic circuit has much in common with the problem of modeling and improving robustness against soft error in digital circuits. In both cases, it is necessary to assess the ability of a circuit to mask any internal miscalculations and to add redundancy ef- fectively. Telecom ParisTech team has developed several methods and tools suitable for these tasks. The thesis work will address the necessary changes to these methods in order to extend their use to probabilistic cir- cuits or, if appropriate, to propose new methods. Indeed, although there is much convergence between the two problems, sources of error are of different natures, and this must be taken into account to obtain relevant results. In addition, we will focus on the impact of these errors in the signal processing operators.

Résumé du projet de recherche (Langue 2)

Scaling of CMOS technologies allowed clock frequency improvement and high-density integration that resulted in wide production of performant com- plex systems on chip (SoC). To reduce the power consumption of such cir- cuits that contain a large number of transistors, it is necessary to reduce the operating voltage. The voltage reduction generates unwanted disturbances that interfere with the signals. Therefore, the logic gates have a probabilis- tic behavior and so produce erroneous results sometimes. In other words, gains in performance, area and power consumption are exchanged by loss of correctness. An important design issue for probabilistic circuits is how to obtain op- timized trade-off between classic design parameters and computing correct- ness. Studies addressing the problem of probabilistic behavior of circuits have been reported in the literature. Similarly, some solutions for correct- ness estimation have been presented. However, these previous work rely on probability models whose relevance is uncertain or produce excessive overcost. In order to do obtain cost-effective implementations, efficient correctness models for probabilistic circuits must be developed. This thesis deals with the development of such models. Another expected contribution of this research are effective mechanisms for increasing the probability of correct results in probabilistic logic circuits.