

Reliability estimation of combinational circuits

Mots clés :

- **Directeur de thèse** : LIRIDA NAVINER
- **Co-encadrant(s)** :
- **Unité de recherche** : Laboratoire Traitement et Communication de l'Information
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Résumé du projet de recherche (Langue 1)

Digital circuits used in such domains as automotive, medical, space or nuclear need to satisfy high reliability requirements. In addition, continuous downsizing of consumer electronics consisting in increased integration and lower voltage supply, affects system's sensitivity to several phenomena involved in transient and permanent faults generation: particle strike, thermal noise, crosstalk, etc. These faults may cause different effects in the system's behavior ranging from silent fault (no effect) to a total loss of functionality. Transient faults in memories and sequential elements have largely dominated the overall soft error rate (SER) of systems, thus, correction and prevention techniques for these devices are well known, and their application is widely spread. Though, it is expected that the contribution of combinational logic elements to the system's SER becomes dominant with CMOS technology downsizing. Hence, there is a need to fulfill the lack of available models and methodologies that take into account the combinational logic's contribution to the reliability loss. Two main approaches exist to assess this issue : fault injection techniques and analytical models. The work of this thesis is focused on the analytical approach, also known as probabilistic approach. First, an in-depth approach of the state of the art methods will be done pointing out the main limitations of probabilistic models. Second, innovative heuristic and approaches will be proposed.