Proposition de recherche doctorale

Defect Tolerance in FPGA

Mots clés :
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- Unité de recherche : Laboratoire Traitement et Communication de l'Information
- École doctorale : École Doctorale Informatique, Télécommunications, Électronique de Paris
- Domaine scientifique principal : Divers

Résumé du projet de recherche (Langue 1)

This research project addresses the problem of designing defect tolerant FPGA. The design context is supposed to be fabless, so no action at physical/mask level is considered. The objective is to propose solutions to achieve this tolerance by implementing strategies that cover architectural and software aspects. The thesis will focus on architecture issues. It means the research of mechanisms for analysis and improving tolerance to faults in BLE (basic logic element), CLE (configurable logic element), S (switch) and C (connection) blocks. The obtained robust basic blocks will be used to construct the defect tolerant FPGA. Also, the improvements achieved at basic blocks level will be used to define the fault tolerance mechanisms required at the FPGA global architecture level.

Résumé du projet de recherche (Langue 2)

FPGAs are becoming increasingly popular thanks to their performance and ability to integrate very complex applications. These circuits have directly benefited from advances in CMOS technology. This progress has resulted in increased integration density according to Moore's Law. However, scaling-down of CMOS devices produces design-induced problems that become a major cause of decrease in manufacturing yield. Because manufacturing yield is a basic parameter in the cost of electronic circuits, its impact is increasingly growing in the trade-offs that the designer must determine. To overcome the problem of reduced yield, various techniques have been developed. Given the increasing complexity of these techniques and their implementation cost in lower levels of abstraction (masks, circuitry), it becomes increasingly costly for the electronics industry to ensure the absence of defects. This leads to a new challenge for designers: they must anticipate the possibility of defects and enhance their design with protective mechanisms against these defects. This PhD project deals with defect tolerant FPGA design suitable for deep submicron technologies. The work is part of Telecom ParisTech activities on reliability of electronic circuits.

Informations complémentaires (Langue 1)

Telecom ParisTech activities on the reliability of electronic circuits are grouped in the NanoElec project. In recent years, the NanoElec project team has developed several partnerships in Europe and Latin America. As a member of the NanoElec project team, the PhD student may benefit from these programs that include both scientific collaboration and funding for student mobility.