Reliability of versatile sigma-delta analog-to-digital converters

Résumé du projet de recherche (Langue 1)
The technology integration for electronics at the nanoscale can further enhance the integration density of digital features, while maintaining the overall consumption of circuits at reasonable levels. This trend is less favorable for analog or mixed-signal circuits. A major innovation is essential to propose and implement new circuits and new architectures for high performance, some techniques standard now proving ineffective. Moreover, it is now very difficult and thus very or too expensive to keep the manufacturing yield at which he was for micrometer technology. It becomes absolutely necessary to incorporate into a method of electronic system design architectures, tools and techniques that will still ensure robust operation, that is to say a high degree of reliability. We propose to analyze the failure mechanisms and to define weighted and sufficiently abstract fault models for architectures of versatile discrete time sigma-delta modulators. The purpose of these models is to study the impact of failures on the functionality and performance. The work will then propose and evaluate, based on the developed models reconfiguration, fault tolerance, self-calibration, self-test and scalability techniques for these converters. Finally, a method will be proposed and evaluated for specifying the architecture of a converter by integrating reliability among the performance criteria.

Résumé du projet de recherche (Langue 2)
The laboratory is currently working on: -* Reliability effects (ageing mostly) modeling of analog functions to get models in Verilog-A/VHDL-AMS -* Definition of an analog front-end design method taking into account the reliability -* The reliability assessment of digital circuits -* Techniques to make digital circuits more robust However, very few works has been done and published up to now on mixed-signal circuits' reliability and particularly on ADC reliability. These works are too general and conceptual to be used in practice. The main challenges are then: -* To model efficiently the ageing and other disturbing effects on a sigma-delta ADC (SDADC) at an abstracted level in order to overcome the complexity and to be able to explore rapidly various potential solutions -* To establish possible compromises between reliability, area, power consumption and other performance criteria as a function of a specific SDADC architecture -* To propose a reliability-aware design method of SDADC

Informations complémentaires (Langue 1)
The laboratory is involved in French, European and international projects (already underway or still candidates) with the reliability thematic as the main or at least an important issue. A stay in a partner laboratory (either industrial or academic) will be implemented if a clear added-value is identified for the current thesis.

Informations complémentaires (Langue 2)
Reliability of integrated circuits in advanced technologies has become today a hot topic. The laboratory is working on reliability issues since 5 years and is now internationally recognized for its know-how and the value of its research on reliability.