Energy efficient memory Architectures using advanced technology nodes

Mots clés :
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Résumé du projet de recherche (Langue 1)
The overall objective of this study is to explore circuit concepts to optimize power consumption and performance of SRAM circuits implemented at advanced technology nodes. This optimization can be achieved at different levels of the SRAM hierarchy: cell, column, bank and memory-cut levels. There are several existing techniques to achieve low-voltage operation and energy optimization. However, co-integration of these techniques without too much overhead at different levels of hierarchy is still missing. These techniques come with new challenges, especially when implemented using advanced technology nodes and for ultra low voltages. The main challenge at advanced technology nodes is the variation in the transistor parameters due to low feature size; while the main bottleneck at ultra-low voltage is performance degradation. Another major concern is that a wide range of VDD operation is required for mobile multi-media applications to achieve energy efficiency. Although intelligent power-aware software exists, making the memory work for wide range-VDD is another challenge. Achievable yield is another challenge at advanced technology nodes (SIP and monolithic 3D integration with the given technology, should be explored for SRAM while taking energy efficiency into the consideration). Our project aims to come up with a methodology to design the circuits addressing the above-mentioned challenges. It aims to fully utilize the merits of the technology (transistors) used for implementation. We plan to work with advanced FD-SOI 20nm process and other technology node design kits available from our current partners. As the research community is making a transition towards Non-volatile memories, we expect this study will fulfill the existing requirements of the SRAM architecture and sensing circuitry in an efficient manner. We expect this work to find widespread use for applications like biomedical electronics and mobile multimedia systems.

Résumé du projet de recherche (Langue 2)
We hope to address the following challenges while maintaining the stable operation of SRAMs: 1. Energy-efficient and variation-tolerant sensing methodology and circuits. 2. Performance improvement at ultra-low voltages through dynamic and adaptive techniques while keeping the power budget into consideration. 3. Variation-tolerant and energy-efficient self-timed control signal generation. 4. SRAM architectures supporting wide VDD range.

Informations complémentaires (Langue 1)
The project plans to involve highly experienced professionals in memory from different parts of the world: ISEP France, BWRC USA, Hitachi Japan and DA-IICT India. Concurrently with this PhD proposal, we are applying for funding to organize the visits and seminars for the first two years through the French Foreign ministry’s STIC-ASIE program. The PhD candidate will work closely with the four persons mentioned, and will be expected to make regular visits abroad.