Contribution à la calibration aveugle de convertisseurs analogiques-numériques entrelacés temporellement

Mots clés :

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Résumé du projet de recherche (Langue 1)

There has been a continued trend in wireless telecommunication standards to increase data rates which has almost been multiplied by one thousand from the early GSM to the latest LTE breakthroughs. The combination of research in digitized and flexible receiver architecture with advances in CMOS process is essential to increase the receiver sampling capability and efficiency which is measured by three criteria: the sampling rate, the resolution and the power consumption. While GSM (2G) used only 200 kHz bandwidth for each channel, carrier aggregation of up to five (non-)contiguous 20MHz channels leading to 100MHz bandwidth must be supporting when considering LTE-Advanced standard (4G). While 14-bits resolution ADCs are needed in conventional 2G narrowband(200kHz) wireless standards to move more baseband filtering functions from analog to digital domain, 10 to 11-bits resolution ADCs are minimum requirement for wideband (100MHz) LTE Advanced standard. In today’s 40/28nm CMOS technology, such speed-resolution products are feasible with acceptable power efficiency only by exploiting the time-domain parallelism of Successive-Approximation-Registerbased (SAR) Analogue-to-Digital Converters (ADCs) interleaved architecture. Time-Interleaved(TI) SAR ADCs are ideally suited to these applications due to their highly scalable architecture, to the steady improvement in matching and density of Metal-Finger Capacitors (MFC) and most of all to the impressive advances in power efficiency. SAR ADCs have reached energies per conversion step below 10fJ. Unfortunately, in time-interleaved architectures, new errors emerge due to the parallelization which imposes significant problems for high-resolution systems. These errors are caused by differences between the individual ADCs used in the time-interleaved ADC system and are commonly referred to as channel mismatch errors. The channel mismatch errors give rise to nonlinear distortion that degrades the resolution. The channel mismatch errors either originate from discrepancies in the time instants when each subconverter is actually taking samples from the analog waveform or differences in how the sampled values are eventually quantized into a digital representation. The most commonly considered mismatch errors are due to static time-skew, gain, offset, jitter, aperture time and bandwidth mismatch. In this work we derive closed form equations for modeling of channel mismatch errors in a Time Interleaved ADCs. This model allow us to separate an ideal part which is due to normal sampling from a disturbing part which comes from discrepancies between the individual interleaved ADCs. This model is used later to derive estimation and correction method which work in tandem. This is calibration. Estimation will consist in identifying the the disturbing part from measurements while correction will consist in proceeding analog feedback and digital post processing in order to reduce as possible the impact of the disturbing part. To avoid time consuming, calibration can be done while the ADC is operating. That's why in this work we propose blind calibration methods which don't need any calibration signal. The main difficulty comes from the fact that we have few informations on the input signal, just a power spectral density or a probability density. We use information theory and statistic methods to resolve this problem. The proposed algorithm(s) will be integrate on a test chip with some exiting Time-Interleave pipeline SAR ADCs on 40 or 28nm CMOS technology.