Résumé du projet de recherche (Langue 1)

This thesis addresses the problem of global synchronization of complex Systems-on-Chip (SOC), e.g. with a multiprocessor SoC. Given the characteristics of modern VLSI technologies, the designer partitions big circuits into many isochronous zones, each one behaving like a classical synchronous circuit. However, with the evolution of modern VLSI technologies, it has become more and more difficult to guarantee global synchronization. Amongst the main reasons one can cite increasing clock frequency together with an increasing circuit complexity, which results in the traditional clock distribution techniques (tree, grid) ceasing to be adequate. Presently, there is growing interest in a solution which consists of getting the circuit blocks to communicate with each other in an asynchronous way (GALS approach, Globally Asynchronous, Locally Synchronous). However, this approach still involves some risks (e.g. metastability…), which can affect the global circuit reliability. In addition, this technique requires special design methods and tools that are very different from those used for the synchronous system design. To circumvent these difficulties, the designers wishing to go on with the Globally Synchronous paradigm, are turning toward clocking techniques, breaking away from classical approaches (e.g. distributed oscillators, stationary waves, coupled oscillators, programmable delays). This study is placed on this research axis. In this research we will study and elaborate a global distributed clocking system for a highly reliable synchronous circuit. This clocking scheme is based on a network of oscillators coupled in phase. Inside each isochronous zone, there is one oscillator that generates the local clock. To synchronize the oscillators, each one of them is provided with a PLL (Phase Locked Loop), realizing a phase coupling between the oscillators of neighboring zones. The work to be done includes the selection of an architecture, the establishment of a theoretical model, an analysis of its behavior, an investigation of the stability conditions of its synchronous operating, the designing blocks for this network and a prototype circuit in a 65 nm STM CMOS technology. (Key words): synchronous clocking, GSLS, multioscillator architecture, all-digital phase locked loop, digitally-controlled oscillator, bang-bang detector, time-to-digital converter