TLM-DT: A MODELING STRATEGY BASED ON DISTRIBUTED TIME FOR PARALLEL SIMULATION OF VIRTUAL MP2SOC PLATFORMS ON SMP WORKSTATIONS

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Résumé du projet de recherche (Langue 1)

Innovative hardware architectures in the microelectronics industry are mainly characterized by their incredibly high level of parallelism. Despite their relative novelty, Multi-Processors System on Chip (MPSoCs) containing a few cores tend to be replaced by Massively Parallel MPSoCs (MP2SoCs), which integrate dozens or hundreds of processor cores interconnected through a possibly hierarchical network on chip. The increase of processing power and parallelism creates the need for faster yet accurate simulation tools for virtual prototyping, supporting both functional verification and performance evaluation (timing and power consumption). Several industrial and academic frameworks appeared to help modeling, simulating and debugging MP2SoC architectures. The SystemC hardware description language is the effective backbone of all these frameworks, which allows to describe the hardware at various levels of abstraction, ranging from synthesizable RTL (more accurate and very slow) to TLM (less accurate and very fast). However, when it comes to simulate an architecture containing hundreds of processors, even the simulation speed brought by TLM is not enough. Simultaneously, multi-core workstations are becoming the mainstream, and SMP (Symmetric Multi-Processors) workstations will soon contain several tens of cores. Unfortunately, the genuine SystemC simulation kernel is fully sequential and cannot exploit the processing power provided by these multi-cores machines. In this context, the strategic goal of this thesis is to propose a general modeling approach for timed TLM virtual prototyping of shared memory MP2SoCs, called Transaction Level Modeling with Distributed Time (TLM-DT). The main idea of the TLM-DT approach is not to use anymore the SystemC global simulation time, becoming possible to use a truly parallel simulation engine and providing a significant reduction in simulation time with a limited loss of precision.