Proposition de recherche doctorale

Non Volatile Random Access Memory Design and Characterization

Mots clés :

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- Co-encadrant(s) :
- Unité de recherche : Laboratoire Traitement et Communication de l'Information
- Ecole doctorale : École Doctorale Informatique, Télécommunications, Électronique de Paris
- Domaine scientifique principal : Divers

Résumé du projet de recherche (Langue 1)

Driven by the demand of mobile applications (phone, tablette, MP3 players…) the market for memories is growing very fast. Today there are 3 mainstream semiconductor memory technologies: SRAM, DRAM and NVM. SRAM (Static-RAM) is characterized by their speed and used as cache for CPUs. DRAM (Dynamic-RAM) is the predominant form of computer memory used off-die in modern computers due to their higher density and lower cost. Both static and dynamic RAM are forms of volatile memory i.e. stored information is lost when power is removed. In contrast NVM (Non-Volatile Memory) enables data to persist without power. NVM is primarily used in memory cards, USB drivers etc. with a market dominated by FLASH products. However NVM has not yet been incorporated into microprocessor or System on Chip (SoC) designs. This is due to long write access time, dynamic power consumption and endurance issues. Recently resistive NVM e.g. CBRAM (Conductive bridge RAM) and OxRAM (Oxide RAM) have gained a lot of attention due to their inherent non-volatility, zero standby leakage power, high density and particularly fast access time (order of nanosecond). These attributes are obviously promising for future high-performance and low-power computing applications. The zero standby leakage current of NVMs makes them very attractive for cache implementation, being the main source of power consumption. Similarly their non-volatility appears very useful for system backup, recovery and error correction circuits.

Résumé du projet de recherche (Langue 2)

The proposed thesis gives the opportunity to challenge new RAM-cache design by taking the best features from resistive RAM memory technology (in particular CBRAM) and implementing them on cache-level. Designing such systems require a deep understanding of NVM device behaviour. The goal of this thesis is also to design a test structure for tracking static and dynamic RAM-cache characteristics and failures. The action plan for the thesis is as follows: -*Study the SRAM, DRAM design caches -*Study the NVM RAM design (NAND/NOR Flash, Hybrid SRAM/RRAM cache, RAM organization…) -*Study the CB/Ox-RAM devices characteristics -*Study the sources of variability and their impact on write-ability and read-ability versus aging -*Push innovative low operating power and high speed ReRAM-cache design solutions considering endurance issues and access time constraints -*Elaborate an efficient and accurate ReRAM-cache test structure for statistical analysis -*Design and tape out a representative demonstrator -*Develop accurate test patterns -*Analyze the dynamic and static data collected -*Extract modeling guidelines for reliability and robustness analysis -*Extract design guidelines for low power and high speed

Informations complémentaires (Langue 1)

The thesis will be held at the heart of the MINATEC innovation campus in LETI laboratories. Pr. Lirida NAVINER, from the Communications & Electronics Department (COMELEC) of Telecom ParisTech, will supervise the thesis. The research work will be done in close collaboration with the Berkeley Wireless Research Center (BWRC) of UC Berkeley and in partnership with ALTIS Semiconductor.

Informations complémentaires (Langue 2)

The supervisors of this work will be -* CEA/LETI: Dr. Olivier THOMAS - olivier.thomas@cea.fr -* TELECOM PARISTECH/COMELEC: Pr. Lirida NAVINER - lirida.naviner@telecom-paristech.fr -* BERKELEY UNIVERSITY/BWRC: Pr. Borivoje NIKOLIC – bora@eecs.berkeley.edu