Design of reliable and low-power digital circuits

Mots clés :

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- Unité de recherche : Laboratoire Traitement et Communication de l'Information
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- Domaine scientifique principal: Divers

Résumé du projet de recherche (Langue 1)

The continuous development of electronic embedded systems comes from the evolution of integrated circuits (ICs) and its design and manufacturing processes [1]. The basic principle behind this evolution is the reduction, or scaling, in the dimensions of the integrated structures. With the current advances achieved in the manufacturing process of integrated circuits, a series of yield and reliability threatening aspects have emerged or have become more prominent [2]. For example, physical defects originating from poorly lithographed wires, vias and other low-level devices are commonly seen in deep sub micron circuits [3]. Circuits have also become more sensitive to the strikes of highly energized particles [4]. On the other hand, in order to keep the power dissipation constantly or at a low degree, the supply voltage should scale with the size [5]. In this situation, the reduction of noise margin makes the transistors and devices working in a noisy signal environment. In other words, the constraints of low power consumption reinforce issues caused by scaling. In consequence, the systems are much more prone to multiple faults and soft errors. Although these phenomena are different, they result in a non-deterministic operation that contributes for lower reliabilities and behaviour uncertainty of embedded electronic systems. In this thesis, we focus on the development of new design methods to cope with these new challenges.

Résumé du projet de recherche (Langue 2)

Several studies are reported in the literature for improving the reliability of circuits [6-9]. Whatever the considered technique, the improvement is accompanied by additional costs. Then, for an enhancement to be effective, it must be obtained at a minimal cost. This efficiency is based on the determination of appropriate metrics for assessing the ratio gain versus penalty. There are several methods and tools for the assessment of penalties (area, speed, power). Nevertheless, the evaluation of the effective gain is a much more complex problem for which existing solutions are not satisfactory [10-12]. Indeed, deep-submicron devices and low-power requirements lead to parametric variability, noise and multiple faults issues that have not yet been simultaneously considered in the reported work. In addition, reliability assessment requires a very high computation effort, which makes actual solutions unsuitable for complex embedded systems. This thesis will focus on the study and development of new approaches for complex architectures assessment in a low power perspective and high reliability while allowing for a cost-effective design. The objective of this thesis is to contribute to new design methods and new architectures for the construction of complex embedded electronic systems based on deep-submicron technologies and under the constraints of fault tolerance and low power consumption.

Informations complémentaires (Langue 1)

Telecom ParisTech and the University of Alberta (Canada) begun a partnership for research in the field of reliable processors design. It is thus expected that the student can benefit from means to make stays within two partner laboratories. This mobility allows the student to take advantage of the resources offered by the two institutions. The PhD student will particularly benefit from the know-how as well as from the methods and tools already developed by the supervisors in the field of reliability analysis and reliability improvement of circuits [13-18].

Informations complémentaires (Langue 2)
References:


