Proposition de recherche doctorale

All-Digital Background Calibration of Timing Skews in undersampling TIADCs

Mots clés :

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- **Unité de recherche** : Laboratoire Traitement et Communication de l'Information
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- **Domaine scientifique principal**: Divers

Résumé du projet de recherche (Langue 1)

Time-Interleaved (TI) of ADCs is a technique to increase the overall system sample rate by using several ADCs in parallel. The challenge is to handle the mismatch between the individual ADCs [1-4], especially at high frequency. The digital calibration of channel and timming mismatches in a TI-ADC has attracted the interest of many researchers during the last decade. The main focus was on the calibration of channel gain [1-4] and timing mismatches [6-10]. Recently, the focus has shifted towards the calibration of FR mismatches [4, 11-14], as this can lead to further improvement in the overall performance of TI-ADCs. In [4] a method to compensate frequency response msimatches based on multi-rate theory and least-squares filter design was presented. The approach works well, however requires special calibration signals, the high filter complexity and extra calibration cycles. A better least-squares filter design method using multichannel filters was presented in [12], but the complexity is still high and the method requires known frequency responses or special input signals to identify them. The correction of bandwidth mismatch for two channel TI-ADC was first introduced in [11], where the correction is basically done as in [4]. A more comprehensive model to correct bandwidth mismatch in a tow channel TI-ADC was developed in [14] which introduces a tailored correction based on a single FIR fitler that channel TI-ADC further reduce the filter complexity. By injecting a test tone of some known frequency below the Nyquist filter, the bandwidth mismatch in a two channel TI-ADC is estimated in an adaptive way. The compensation of frequency response mismatches by using polynomial representations has been investigated in [16-17]. [18-19] presented a blind calibration structure based on a multi-rate filter bank for a two channel TI-ADC. In [16] a compensation structure based on the polynomial approximate frequency response mismatches was introduced. The proposed structure uses differentiators and variable multipliers corresponding to the parameters in polynomial models of the channel frequency responses. Comparing to the state of the art, our works for example in [8] take into account the implementation constraints. Not only theoretical study, modeling and simulations were carried out, but algorithms and digital techniques is tested in FPGA platform at very high frequency rate (>2.5GHz), the optimization of computing resource and power consumption is the key metrics in our approach. Another challenge of wideband ADC in general and TI-ADCs in particular is the non linearities which limit the dynamic range of the ADC, especially in TI-ADC where low order on-linearities are from interleaving and non-linearities caused by pre-ADC anaolog components (such as, amplifiers, filters, buffers, and Smaple/hold). In this project, we will propose digital techniques for the post-processing of the output from TI-ADCs that enhances the linearity of the TI-ADC. It compensate static non-linearities and frequency dependent non-linearities and improves the dynamic range.

Résumé du projet de recherche (Langue 2)

The objective is to handle the mismatch between the individual ADCs, especially at high frquencies. In TI-ADCs, the idea is to correct the manufacturing variations of the chracteristics fo the individual channel ADC in order to obtain the optimal resolution. The variations after correction must be less than 0.01% in order to achieve the successful interleaving of a typical 14-bit ADC. Futhermore, these variations depend on temperature and age, making the corrections required even more complex. In order to reduce mismatch effect, we propose background of frequency-dependent channel mismatch (gian, offset and bandwidth) and time skew error corrections without the need for any special calibration signal or post-production strimming. Another challenge for wideband ADCs in general and TI-ADCs in particular is the non-linearities. In TI-ADCs, non-linearities are from interleaving and pre-ADC analog components (such as amplifiers, filters, buffers, and Sample&Hold). They significantly reduce the dynamic range, SNDR and SFDR of TI-ADC. In this thesis, we propose digital techniques for the post precessing the output of TI-ADC that enhance s the non-linearities and improve the dynamic range of the ADC. The objective is to attenuate the second and third order distortion spurs to the noise floor level and that the usable bandwidth is extended up to 5th Nyquist Zone. Because the digital calibration and linearization techniques will run high frequency rates (>2.5GHz), they will be optimized and adapted under low power consumption and limited computing resource. An implementation on ASIC for validation and performance evaluation will be carried out at the last stages of project. The expected results will boost performance of the TI-ADC to 70dB of dynamic range and more than 10bits of effective resolution at more than 2.5 GHz of frequency rates. The number of channels is up to 64. The power consumption for the digital calibration and correction is under 180mW in 1.2V 65nm CMOS Technology.