Performance optimization on GPU & SIMD for the LHCb experiment

Mots clés :
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Résumé du projet de recherche (Langue 1)
The LHCb Upgrade programme will bring many improvements to the existing detector: in additions to the hardware changes, the LHCb collaboration is planning to fully reconstruct the events in real time and to deploy a trigger implemented in software, using off-the-shelf hardware. This implies tracking the particles in the detector and filtering events at a frequency of 30MHz, using computing resources of the same order as today. Making optimal use of the computing resources available, and investigating alternative architectures are therefore crucial to this endeavour. The candidate will investigate the computational problems encountered: first the data preparation from the raw detector format to one suitable for for physics processing, and in a second phase the rewrite (or the design of new algorithms) of the combinatorics engine that matches the events to requested particle decays chains in the second level trigger. Goals: She/He will explore the algorithms suitable to solve those problems, as well as their adequation to the state-of-the-art parallel architectures (multi-core SIMD general purpose processor, GPU), in order to choose the best solution of the LHCb Online farm. Moreover, if a straight-forward parallelization is inefficient to leverage all the computation power (memory bandwidth issue), the candidate will focus on memory layout optimizations and data management in order to design algorithm with a better throughput. Finally the architectures will be challenged together to determine what is the most appropriate architecture for each type of algorithms. This should guide the design of the new global architecture One of the first algorithm to redesign is the connected component labeling and analysis algorithm that provide a unique label for each binary component. Such an algorithm is used in the early steps of detectors.